//testbench

module decoder3to8tb;

reg [2:0] inp;

wire [7:0] out;

decoder3to8 uut(.inp(inp), .out(out));

initial begin

$dumpfile("decoder3to8.vcd");

$dumpvars(1);

inp = 3'b010;

#100;

inp = 3'b001;

#100;

inp = 3'b100;

#100;

inp = 3'b111;

#100;

$finish;

end

endmodule

//design

module decoder3to8(inp, out);

input [2:0] inp;

output reg [7:0] out;

always @\* begin

case (inp)

3'b000: out = 8'b00000001;

3'b001: out = 8'b00000010;

3'b010: out = 8'b00000100;

3'b011: out = 8'b00001000;

3'b100: out = 8'b00010000;

3'b101: out = 8'b00100000;

3'b110: out = 8'b01000000;

3'b111: out = 8'b10000000;

endcase

end

endmodule